APPROVED BY DRAFTSMAN | O.G. FIG. CLASS SUBCLASS

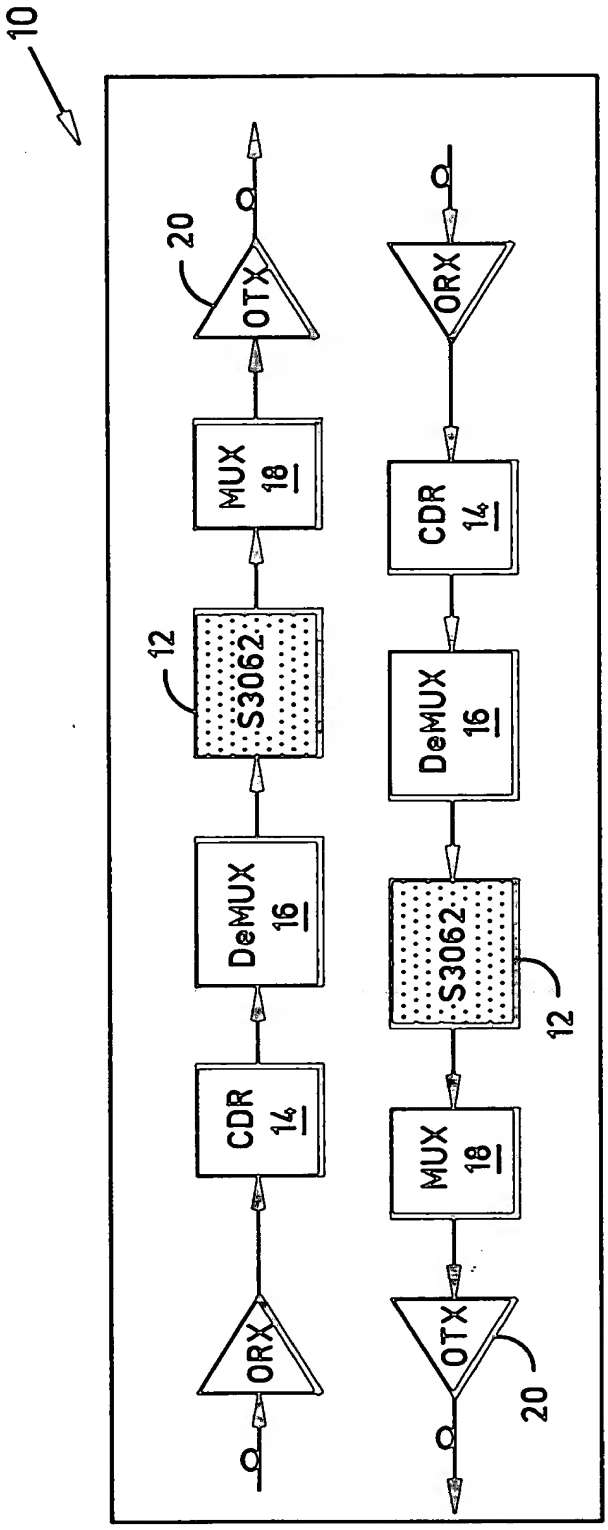

FIG. 1

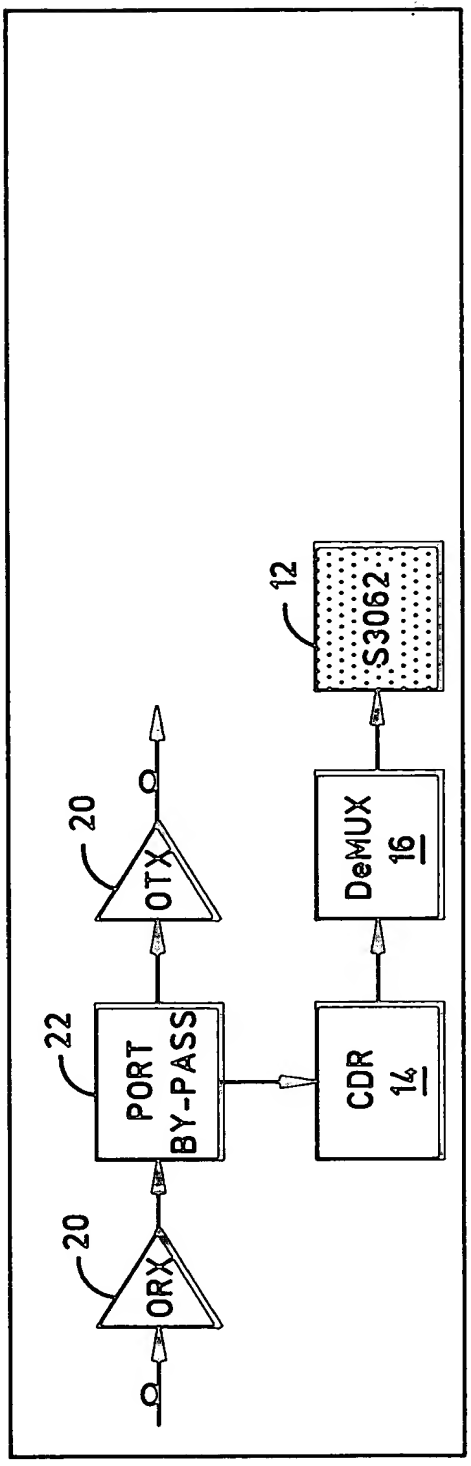

FIG. 2

APPROVED O.G. FIG.
BY CLASS SUBCLASS
DRAFTSMAN

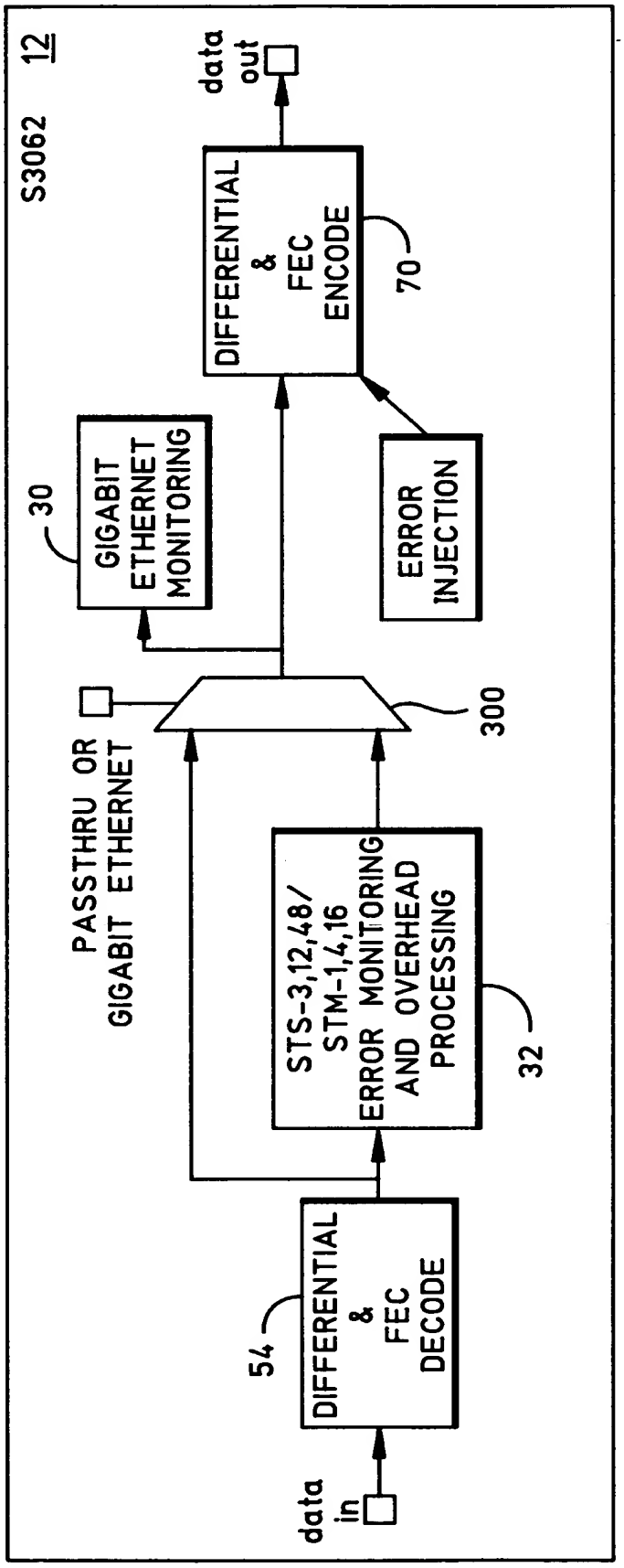

FIG. 3

APPROVED O.G. FIG.
BY CLASS SUBCLASS
DRAFTSMAN

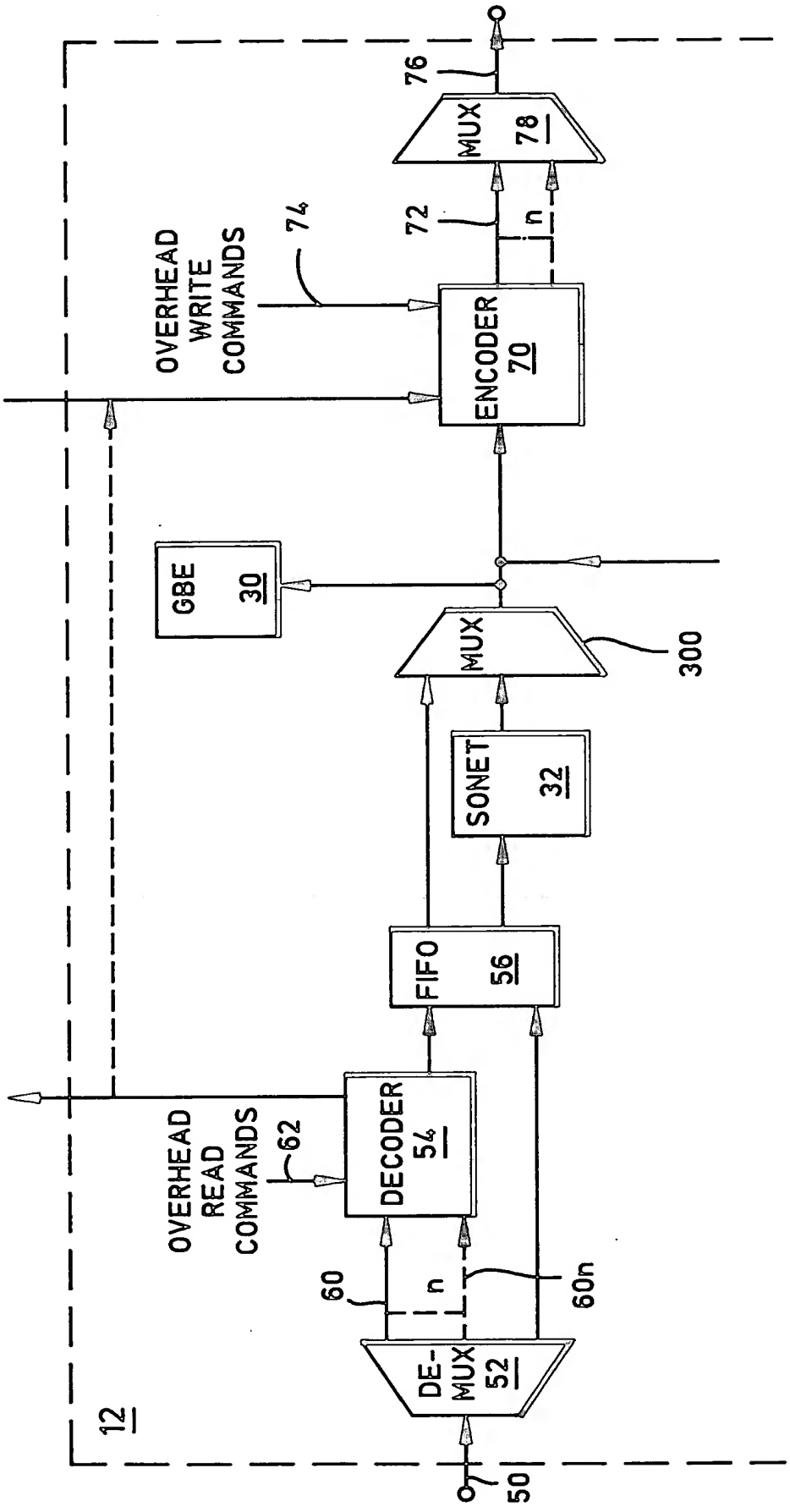

FIG. 4A

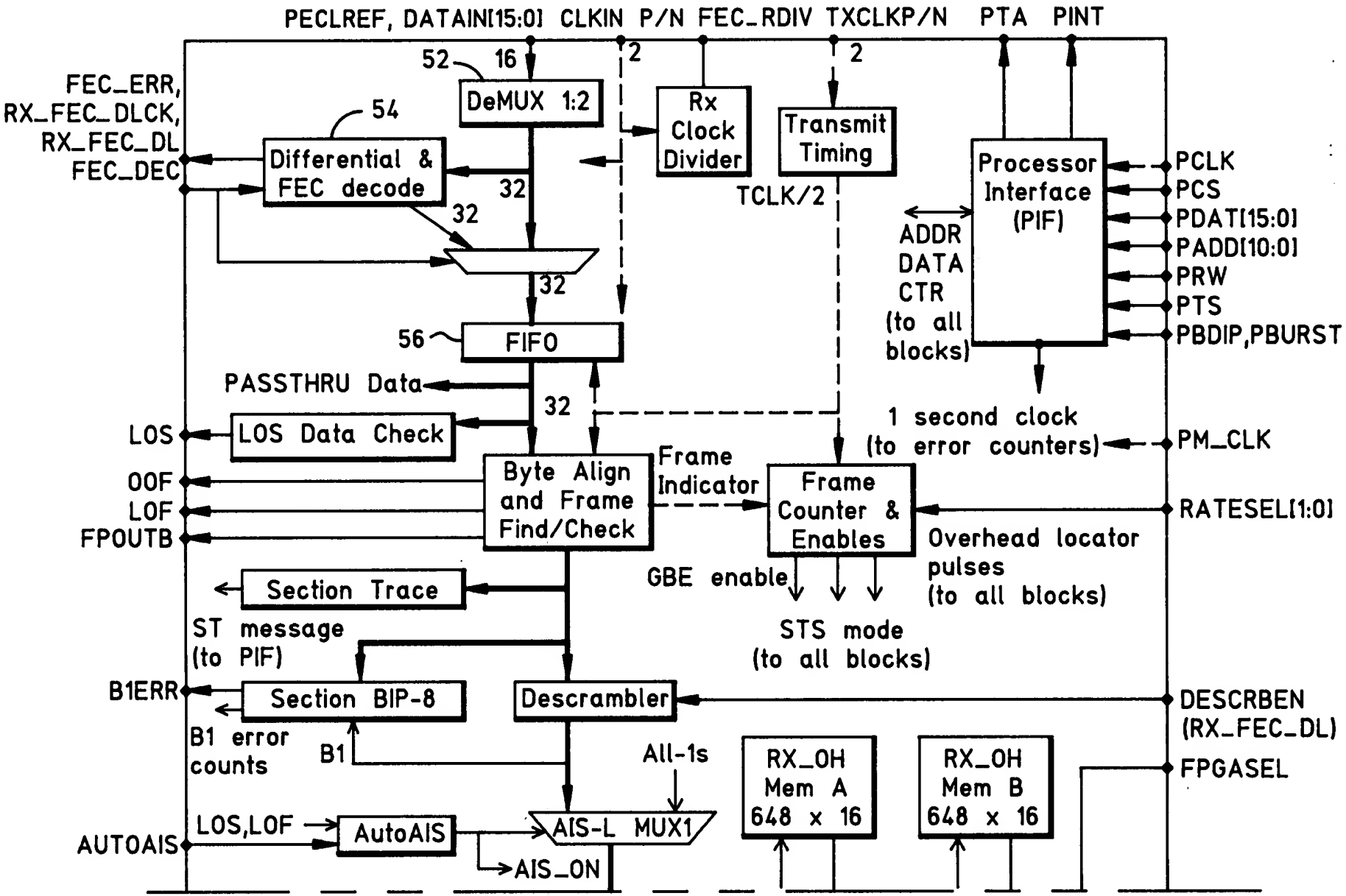
PECLREF, DATAIN[15:0] CLKIN P/N FEC_RDIV TXCLKP/N PTA PINT
52
16
2
2
DeMUX 1:2
Rx Clock Divider
Transmit Timing
Processor Interface (PIF)
FEC_ERR,
RX_FEC_DLCK,
RX_FEC_DL
FEC_DEC
54
Differential & FEC decode
32
32
32
TCLK/2
ADDR
DATA
CTR
(to all blocks)
PCLK
PCS
PDAT[15:0]
PADD[10:0]
PRW
PTS
PBDIP,PBURST
56
FIFO
PASSTHRU Data
32
LOS
LOS Data Check
1 second clock
(to error counters)
PM_CLK
OOF
LOF
FPOUTB
Byte Align and Frame Find/Check
Frame Indicator
Frame Counter & Enables
RATESEL[1:0]
Overhead locator pulses
(to all blocks)
GBE enable
STS mode
(to all blocks)
Section Trace
ST message
(to PIF)
B1ERR
Section BIP-8
Descrambler
DESCRBEN
(RX_FEC_DL)
B1 error
counts
B1
All-1s
RX_OH
Mem A
648 x 16
RX_OH
Mem B
648 x 16
FPGASEL
LOS,LOF
AUTOAIS
AutoAIS
AIS-L MUX1
AIS_ON

FIG. 4B1

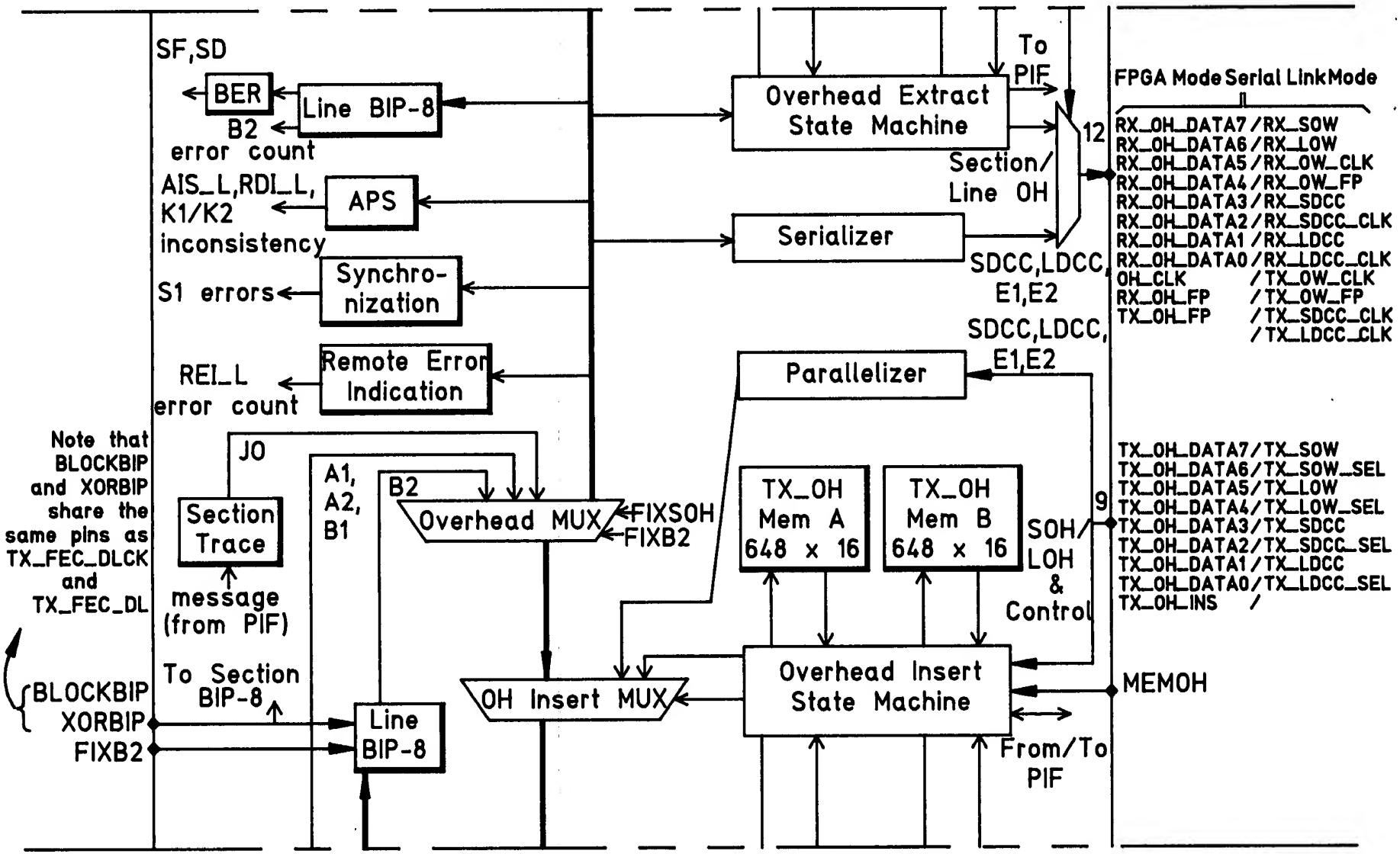
SF,SD
BER
Line BIP-8
B2
error count
AIS_L,RDI_L,
K1/K2
inconsistency
APS
S1 errors
Synchro-
nization
REI_L
error count
Remote Error
Indication
Note that
BLOCKBIP
and XORBIP
share the
same pins as
TX_FEC_DLCK
and
TX_FEC_DL
J0
Section
Trace
message
(from PIF)
A1,
A2,
B1
B2
Overhead MUX
FIXSOH
FIXB2
To Section
BIP-8
BLOCKBIP
XORBIP
FIXB2
Line
BIP-8
OH Insert MUX
Overhead Extract
State Machine
To
PIF
Section/
Line OH
12
Serializer
SDCC,LDCC,
E1,E2
SDCC,LDCC,
E1,E2
Parallelizer
TX_OH
Mem A
648 x 16
TX_OH
Mem B
648 x 16
SOH/
LOH
&
Control
9
Overhead Insert
State Machine
From/To
PIF
MEMOH
FPGA Mode Serial Link Mode
RX_OH_DATA7 /RX_SOW
RX_OH_DATA6 /RX_LOW
RX_OH_DATA5 /RX_OW_CLK
RX_OH_DATA4 /RX_OW_FP
RX_OH_DATA3 /RX_SDCC
RX_OH_DATA2 /RX_SDCC_CLK
RX_OH_DATA1 /RX_LDCC
RX_OH_DATA0 /RX_LDCC_CLK
OH_CLK /TX_OW_CLK
RX_OH_FP /TX_OW_FP
TX_OH_FP /TX_SDCC_CLK
/TX_LDCC_CLK
TX_OH_DATA7/TX_SOW
TX_OH_DATA6/TX_SOW_SEL
TX_OH_DATA5/TX_LOW
TX_OH_DATA4/TX_LOW_SEL
TX_OH_DATA3/TX_SDCC
TX_OH_DATA2/TX_SDCC_SEL
TX_OH_DATA1/TX_LDCC
TX_OH_DATA0/TX_LDCC_SEL
TX_OH_INS /

FIG. 4B2

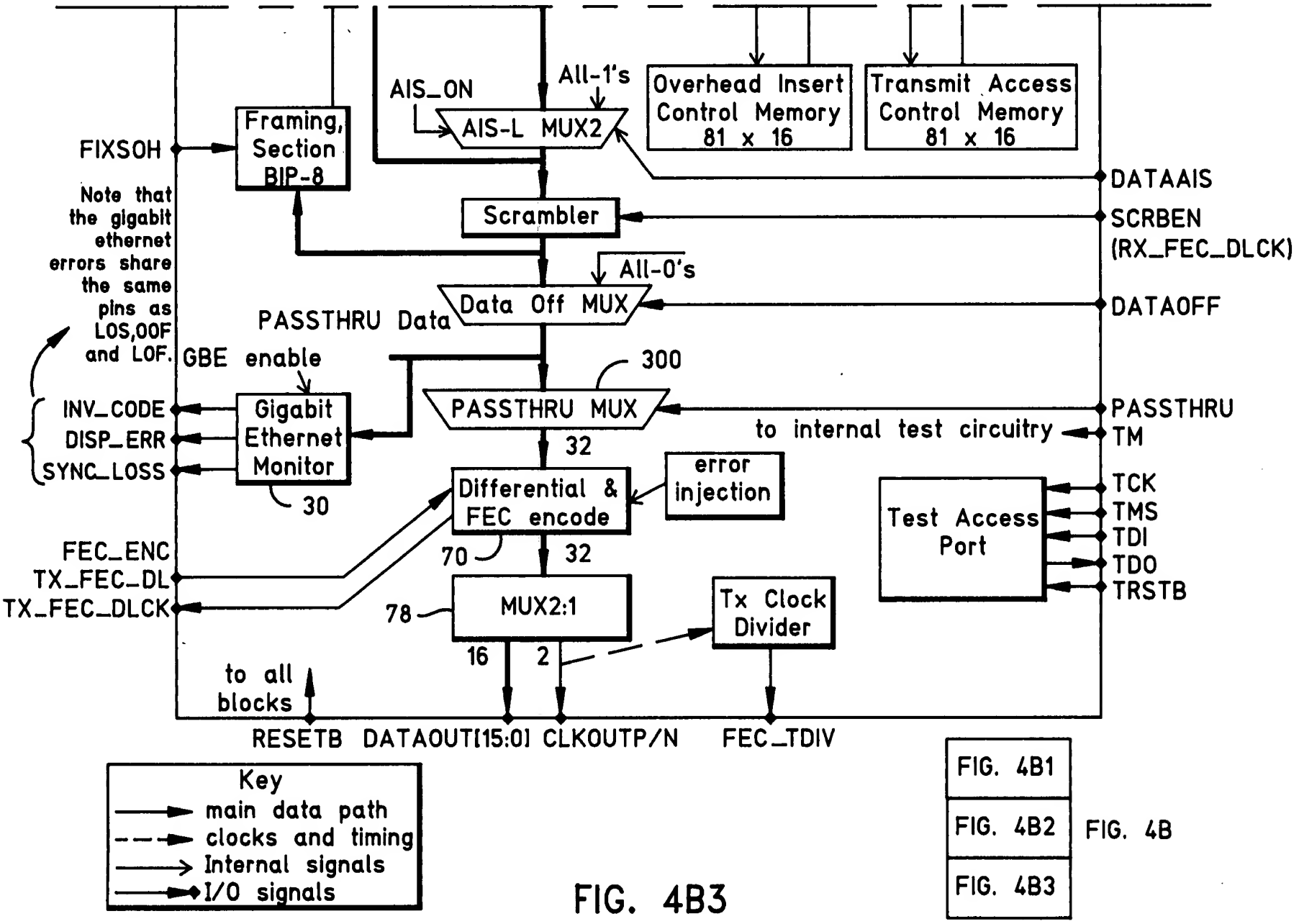

FIG. 4B3

FIG. 4B1
FIG. 4B2
FIG. 4B3
FIG. 4B

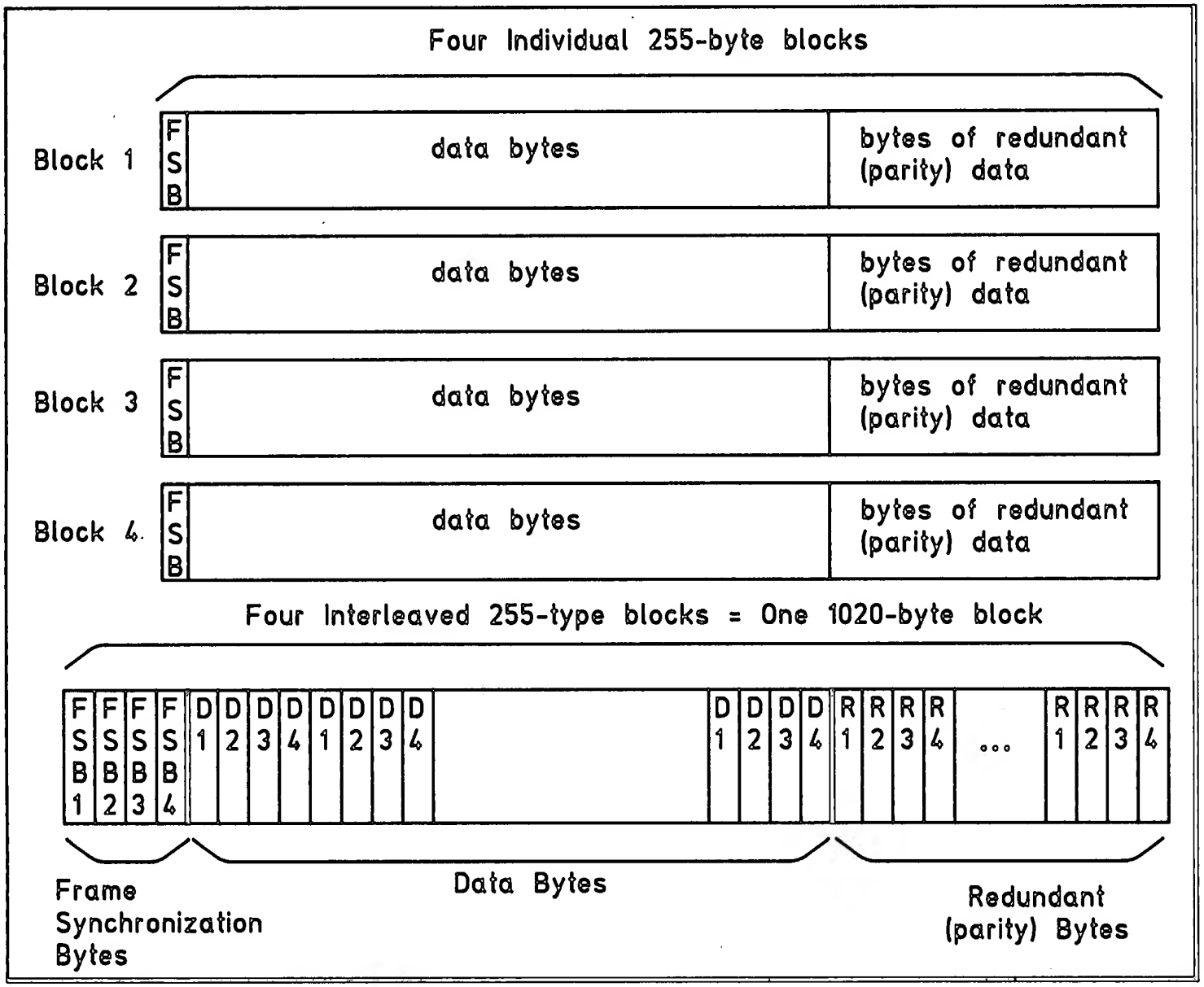
Four Individual 255-byte blocks
Block 1
FSB
data bytes
bytes of redundant (parity) data
Block 2
FSB
data bytes
bytes of redundant (parity) data
Block 3
FSB
data bytes
bytes of redundant (parity) data
Block 4
FSB
data bytes
bytes of redundant (parity) data
Four Interleaved 255-type blocks = One 1020-byte block
FSB1 FSB2 FSB3 FSB4 D1 D2 D3 D4 D1 D2 D3 D4 D1 D2 D3 D4 R1 R2 R3 R4 ... R1 R2 R3 R4
Frame Synchronization Bytes
Data Bytes
Redundant (parity) Bytes

FIG. 5

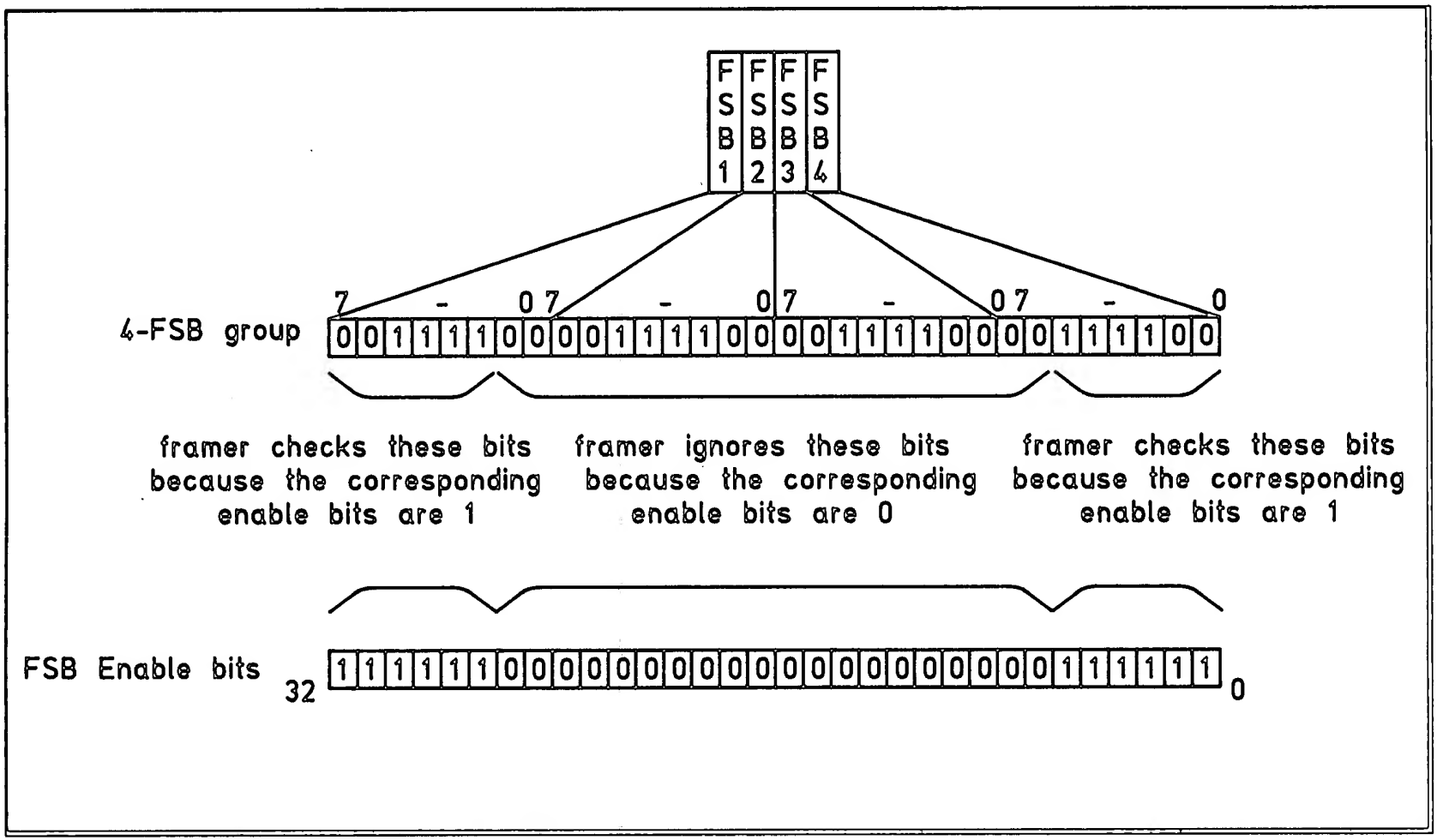
FSB1
FSB2
FSB3
FSB4
4-FSB group
7 - 0 7 - 0 7 - 0 7 - 0
0 0 1 1 1 1 0 0 0 0 1 1 1 1 0 0 0 0 1 1 1 1 0 0 0 0 1 1 1 1 0 0
framer checks these bits because the corresponding enable bits are 1
framer ignores these bits because the corresponding enable bits are 0
framer checks these bits because the corresponding enable bits are 1
FSB Enable bits
32
1 1 1 1 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 1
0

FIG. 6

APPROVED O.G. FIG.
CLASS

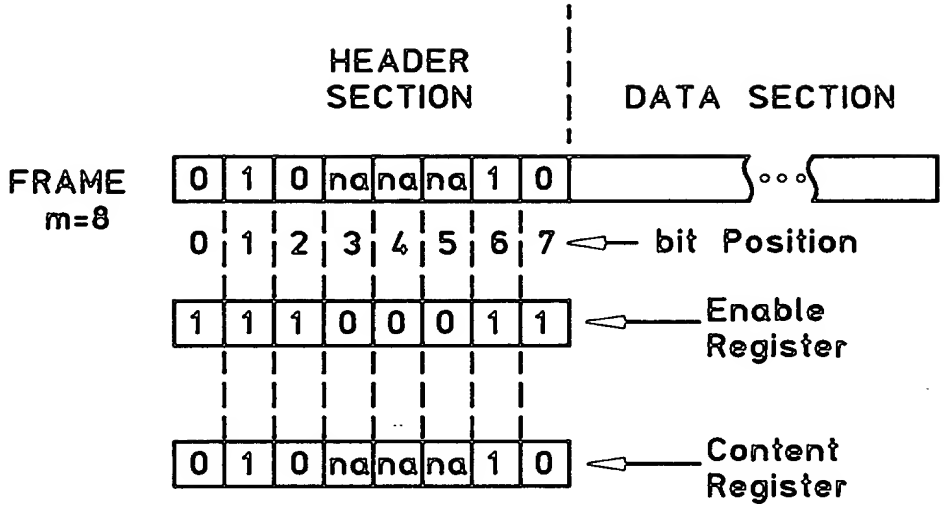

FIG. 7

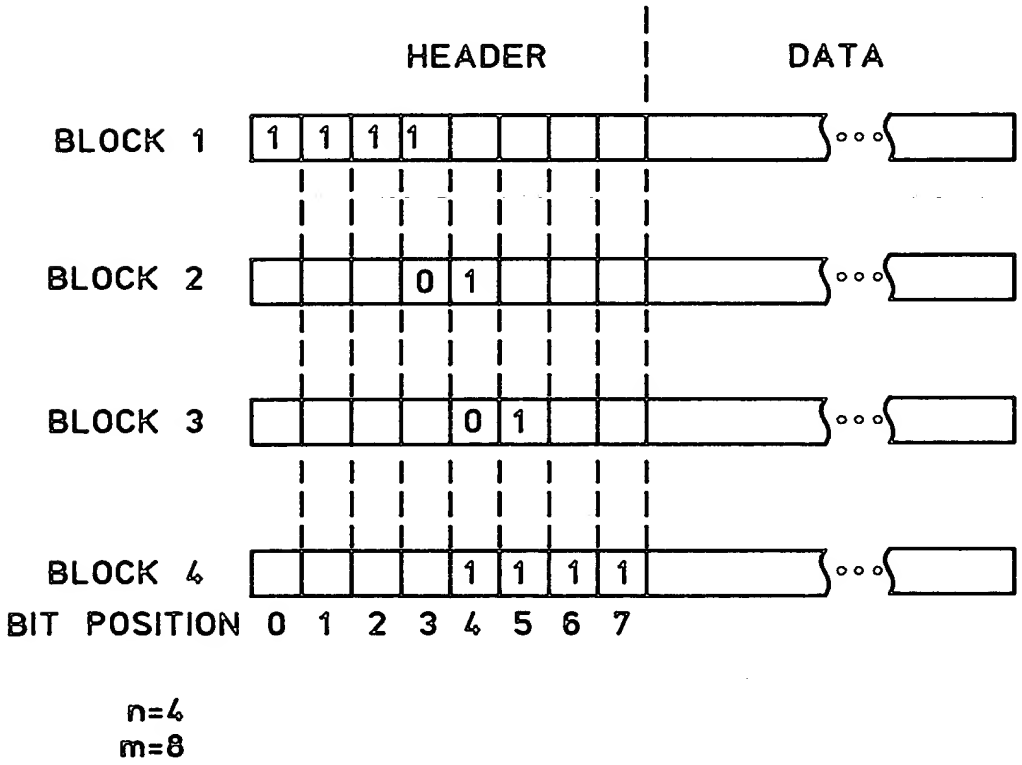

FIG. 8

CLASS SUBCLASS

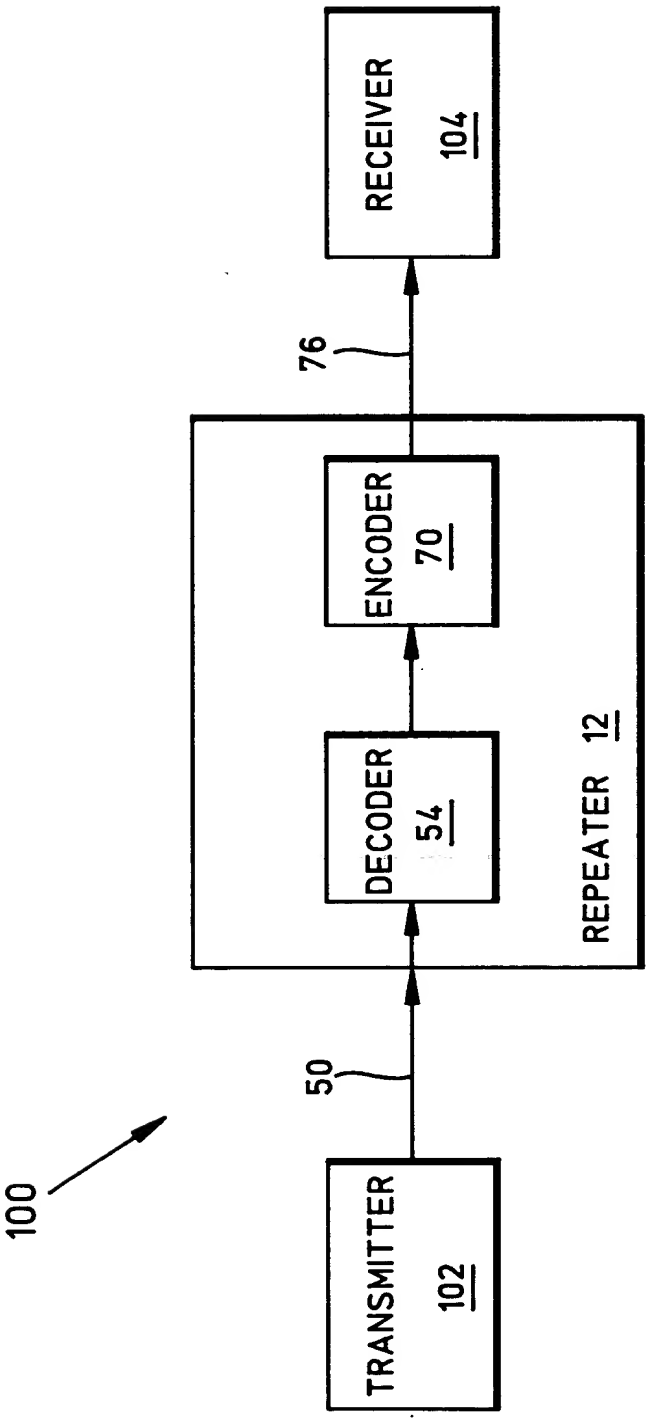

FIG. 9

CLASS SUBCLASS

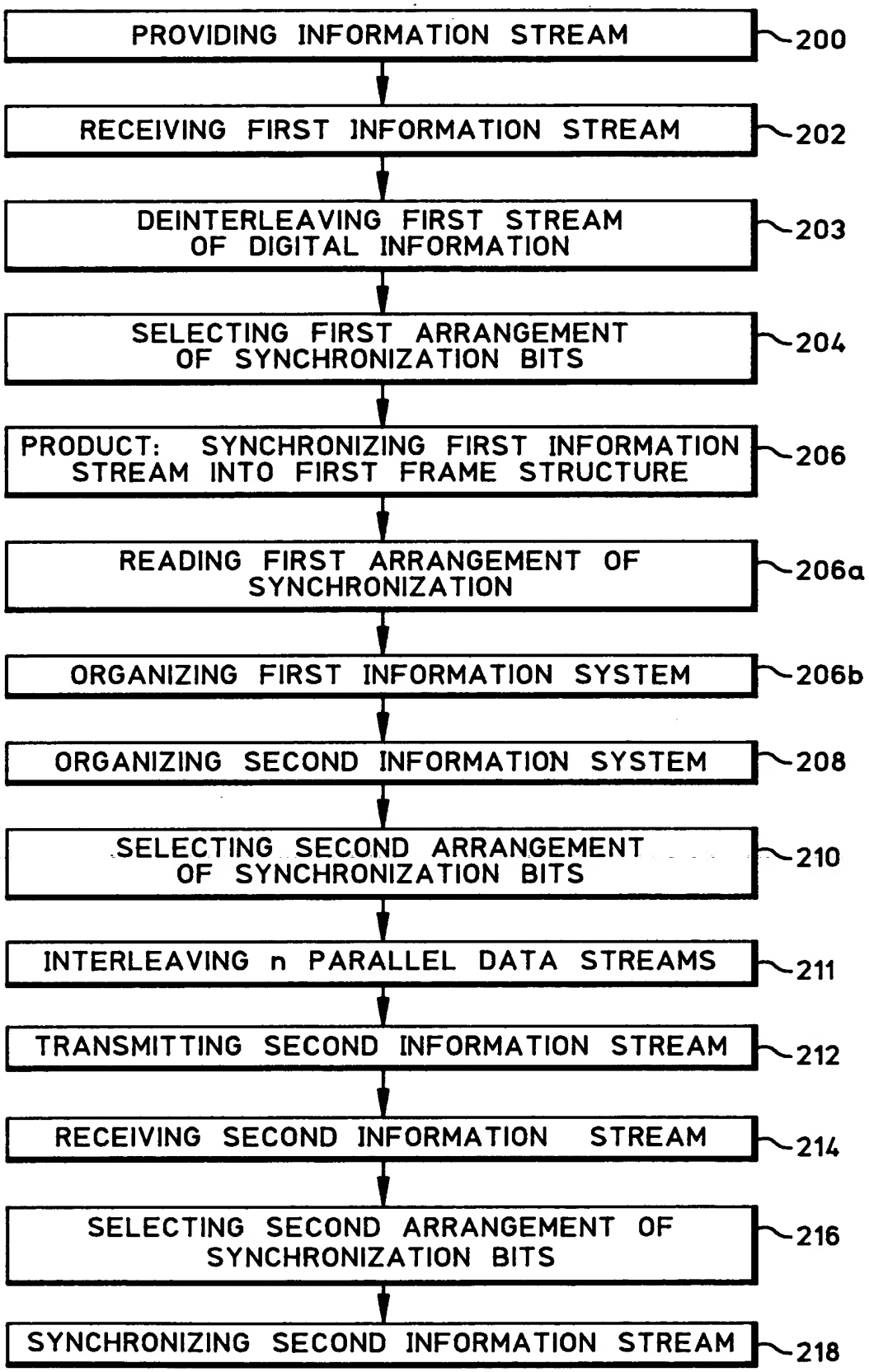

FIG. 10

CLASS SUBCLASS

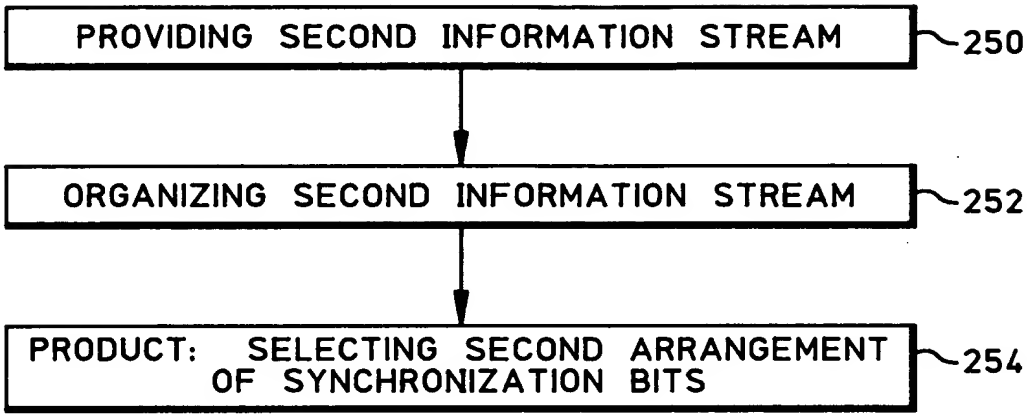

FIG. 11

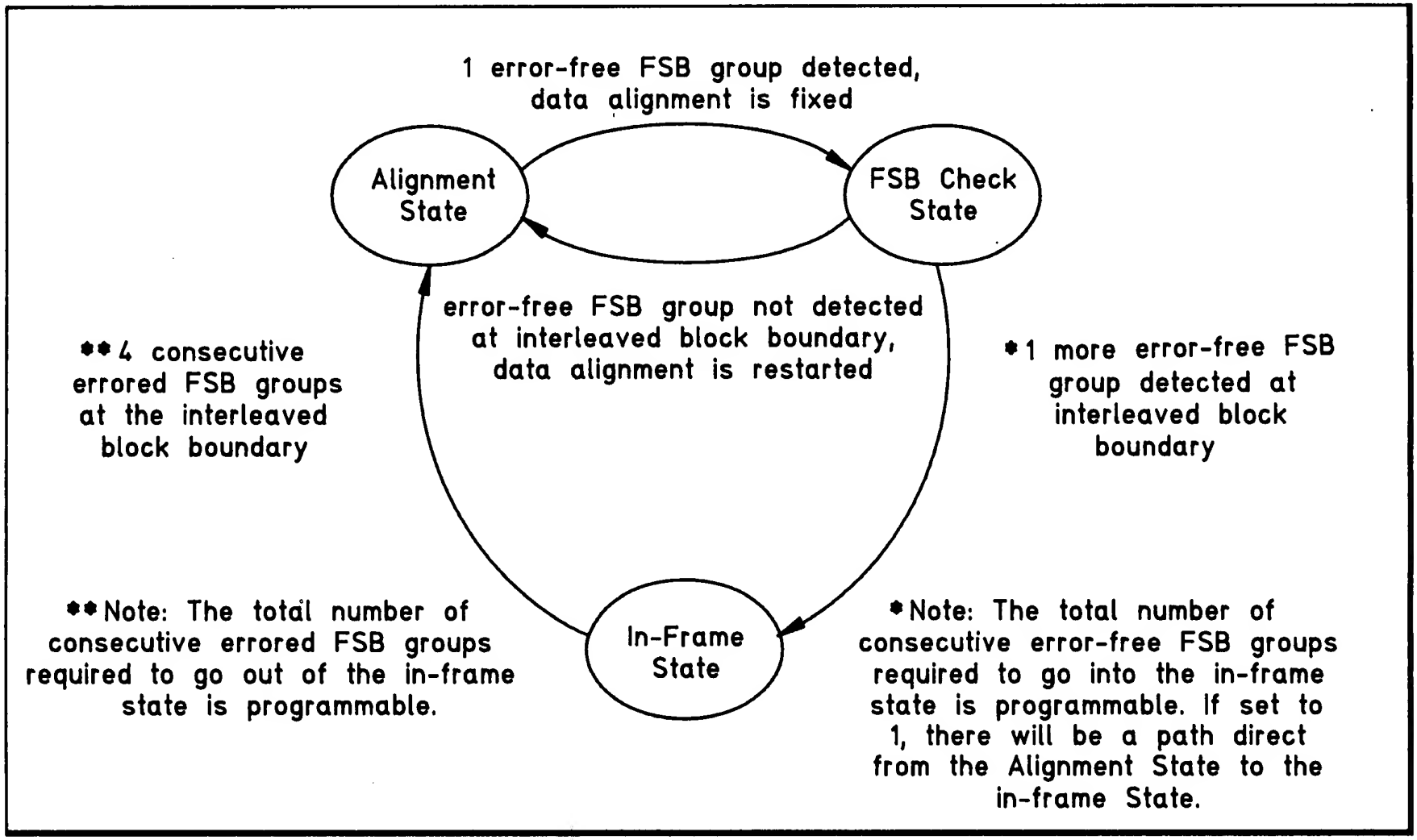
1 error-free FSB group detected, data alignment is fixed
Alignment State
FSB Check State
error-free FSB group not detected at interleaved block boundary, data alignment is restarted
**4 consecutive errored FSB groups at the interleaved block boundary
*1 more error-free FSB group detected at interleaved block boundary
In-Frame State
**Note: The total number of consecutive errored FSB groups required to go out of the in-frame state is programmable.
*Note: The total number of consecutive error-free FSB groups required to go into the in-frame state is programmable. If set to 1, there will be a path direct from the Alignment State to the in-frame State.

FIG. 12

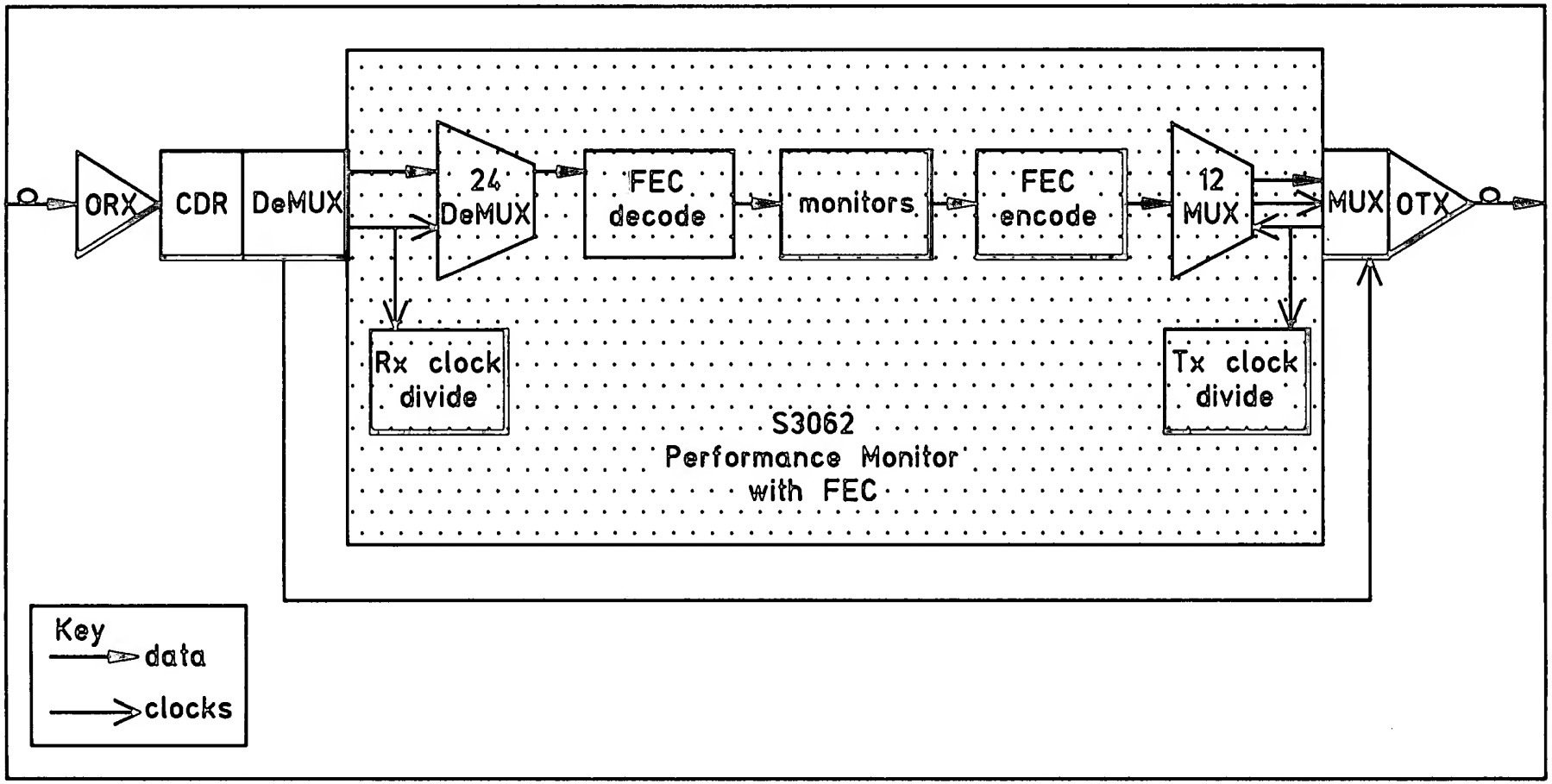
ORX
CDR
DeMUX
24
DeMUX
FEC
decode
monitors
FEC
encode
12
MUX
MUX
OTX
Rx clock
divide
Tx clock
divide
S3062
Performance Monitor
with FEC
Key
data
clocks

FIG. 13

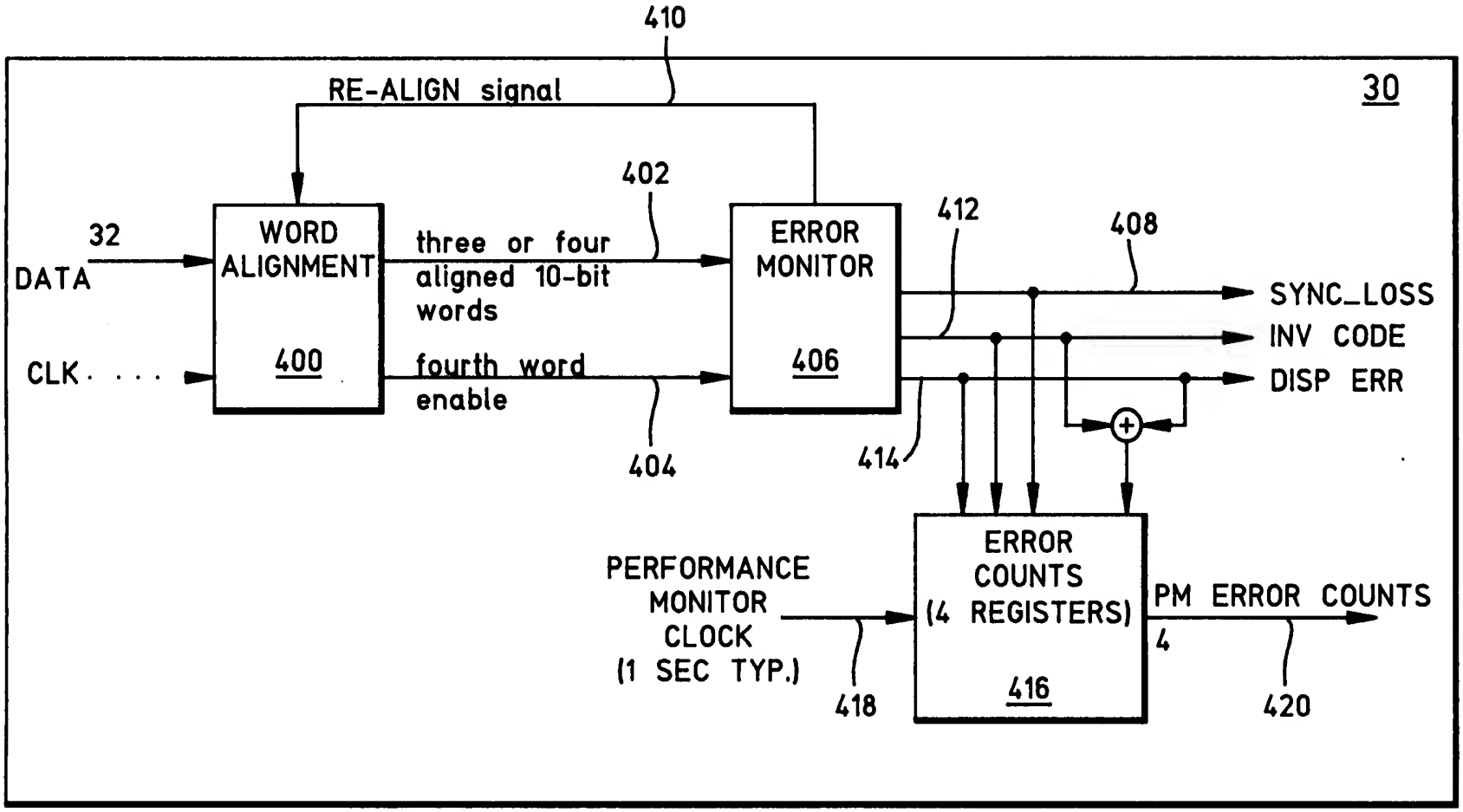
410
RE-ALIGN signal
30
402
32
DATA
WORD
ALIGNMENT
400
three or four
aligned 10-bit
words
ERROR
MONITOR
406
412
408
SYNC_LOSS
INV CODE
DISP ERR
CLK
fourth word
enable
404
414
ERROR
COUNTS
(4 REGISTERS)
416
PERFORMANCE
MONITOR
CLOCK
(1 SEC TYP.)
418
PM ERROR COUNTS
4
420

FIG. 14

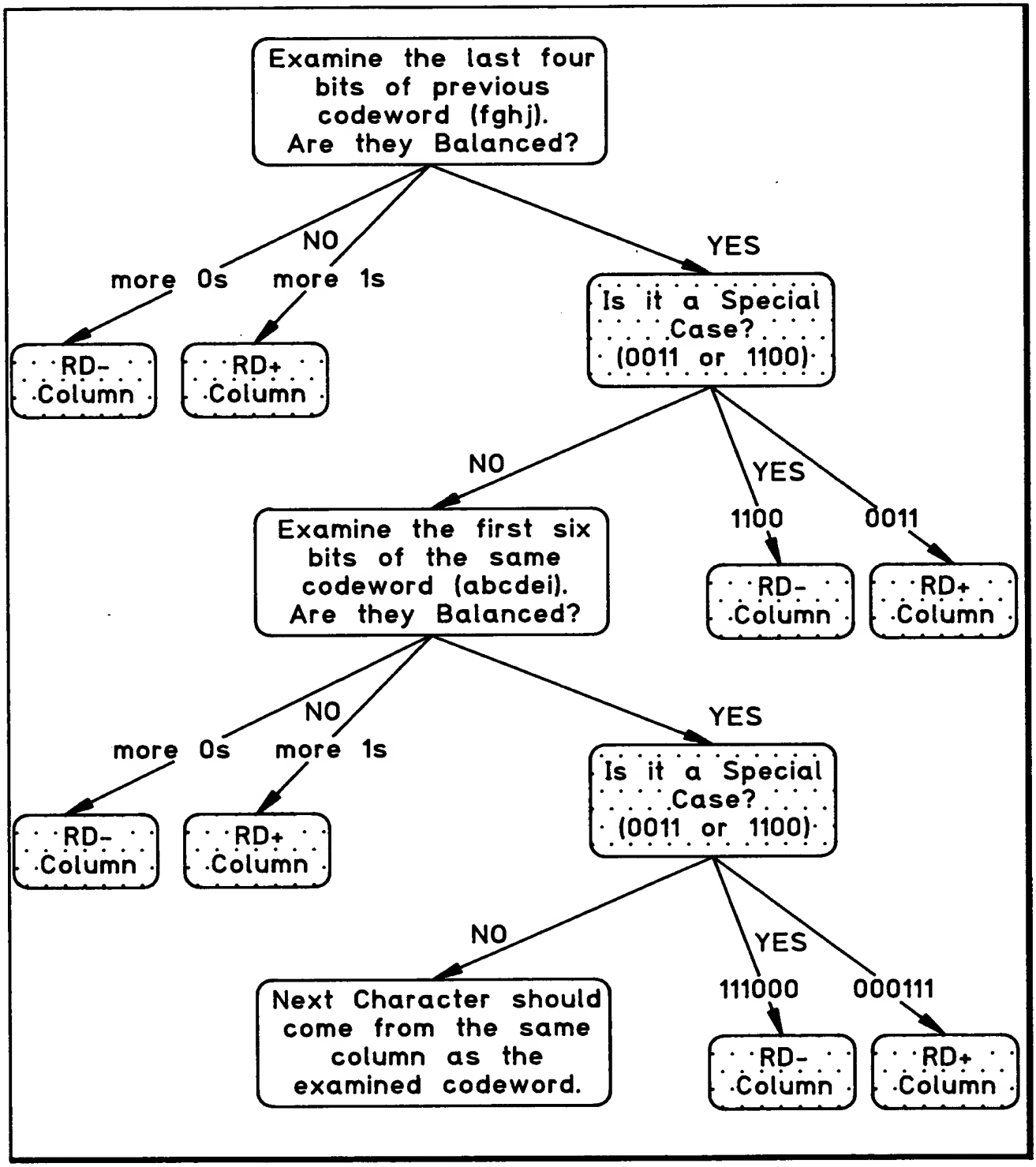
Examine the last four bits of previous codeword (fghj). Are they Balanced?
NO
YES
more 0s
more 1s
RD- Column
RD+ Column
Is it a Special Case? (0011 or 1100)
NO
YES
1100
0011
Examine the first six bits of the same codeword (abcdei). Are they Balanced?
RD- Column
RD+ Column
NO
YES
more 0s
more 1s
RD- Column
RD+ Column
Is it a Special Case? (0011 or 1100)
NO
YES
111000
000111
Next Character should come from the same column as the examined codeword.
RD- Column
RD+ Column

FIG. 15

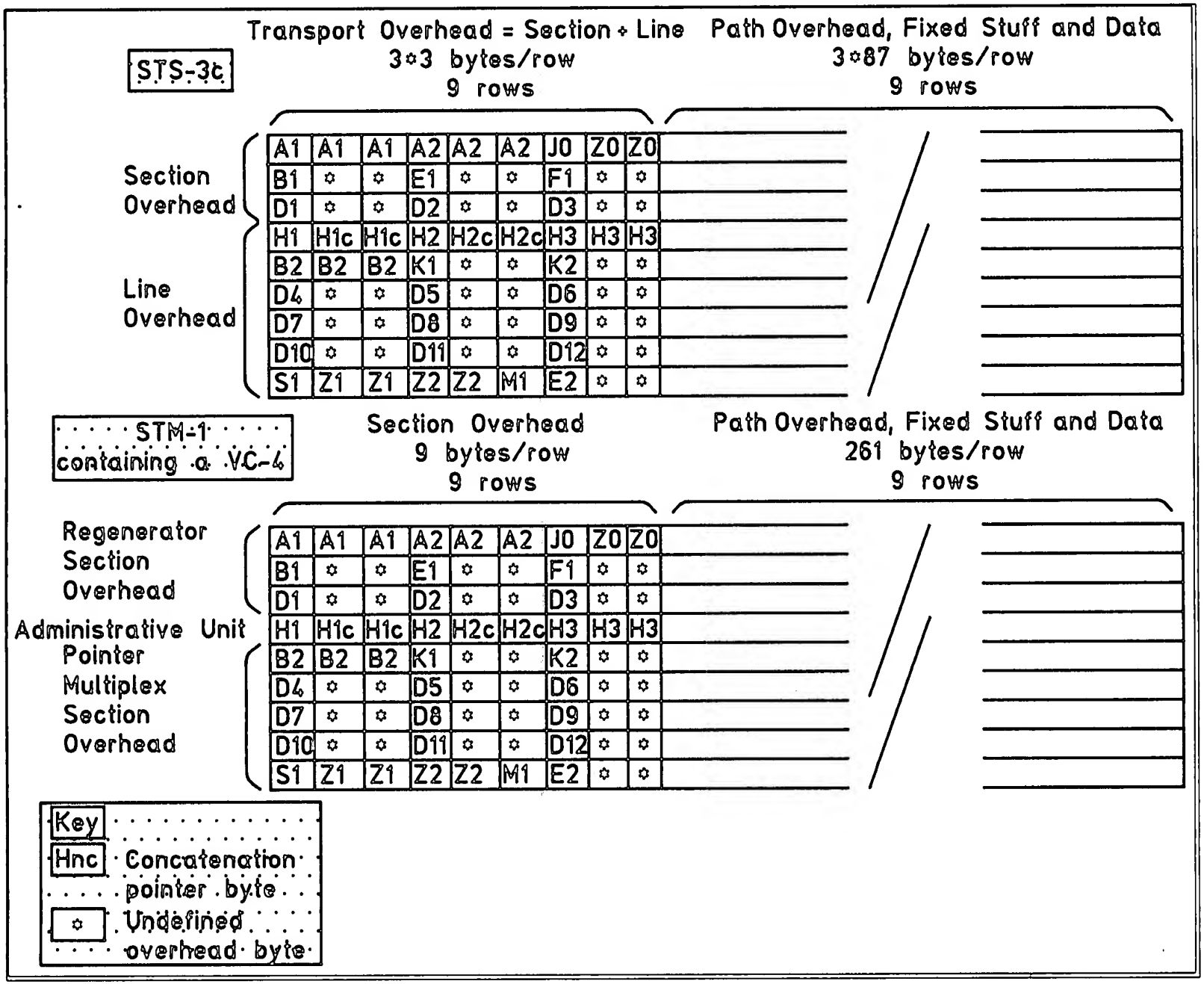
STS-3c
Transport Overhead = Section + Line
3*3 bytes/row
9 rows
Path Overhead, Fixed Stuff and Data
3*87 bytes/row
9 rows
Section Overhead
Line Overhead
A1 A1 A1 A2 A2 A2 J0 Z0 Z0
B1 * * E1 * * F1 * *
D1 * * D2 * * D3 * *
H1 H1c H1c H2 H2c H2c H3 H3 H3
B2 B2 B2 K1 * * K2 * *
D4 * * D5 * * D6 * *
D7 * * D8 * * D9 * *
D10 * * D11 * * D12 * *
S1 Z1 Z1 Z2 Z2 M1 E2 * *
STM-1 containing a VC-4
Section Overhead
9 bytes/row
9 rows
Path Overhead, Fixed Stuff and Data
261 bytes/row
9 rows
Regenerator Section Overhead
Administrative Unit Pointer
Multiplex Section Overhead
A1 A1 A1 A2 A2 A2 J0 Z0 Z0
B1 * * E1 * * F1 * *
D1 * * D2 * * D3 * *
H1 H1c H1c H2 H2c H2c H3 H3 H3
B2 B2 B2 K1 * * K2 * *
D4 * * D5 * * D6 * *
D7 * * D8 * * D9 * *
D10 * * D11 * * D12 * *
S1 Z1 Z1 Z2 Z2 M1 E2 * *
Key
Hnc Concatenation pointer byte
* Undefined overhead byte

FIG. 16

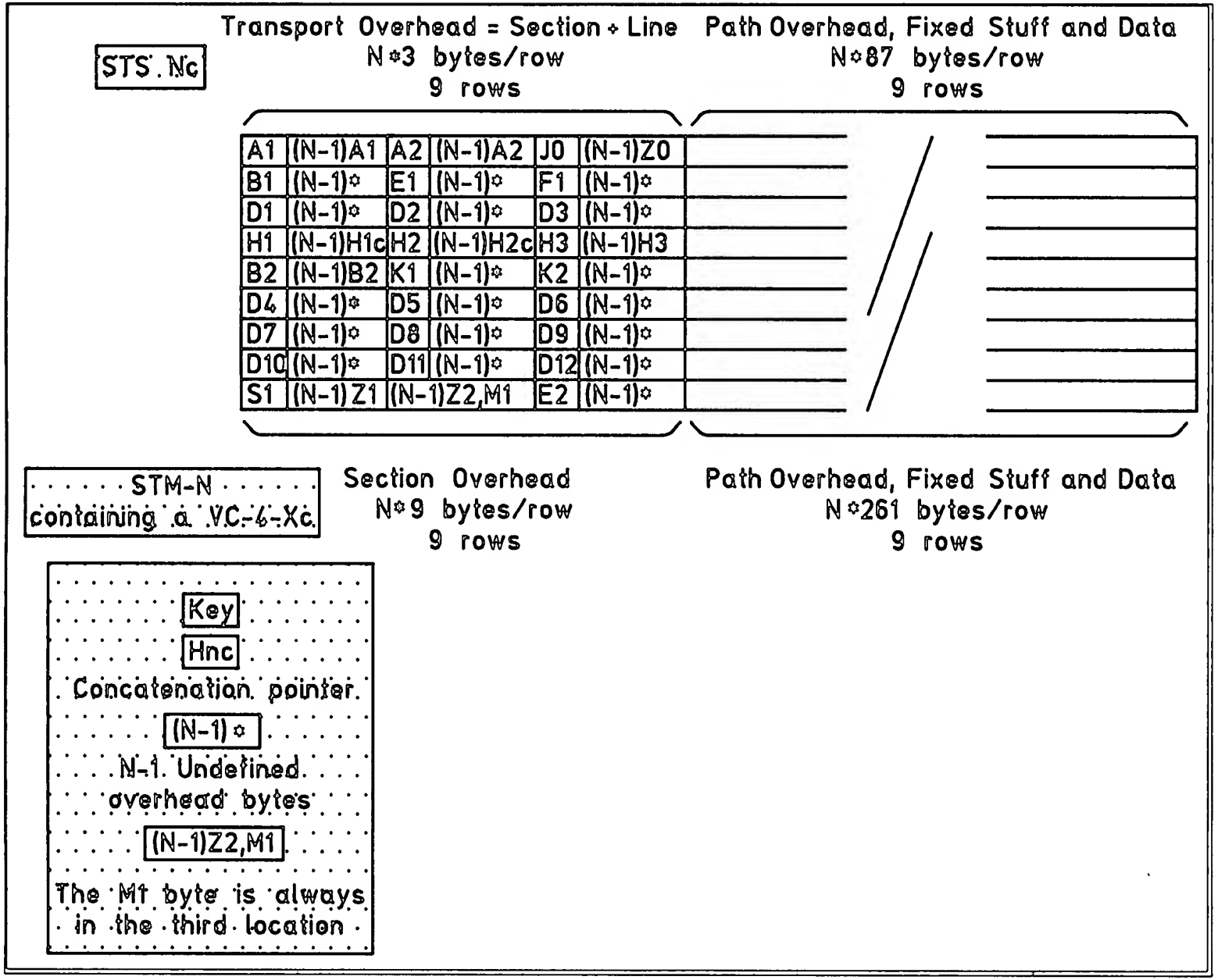
STS-Nc
Transport Overhead = Section + Line
N*3 bytes/row
9 rows
Path Overhead, Fixed Stuff and Data
N*87 bytes/row
9 rows
A1 (N-1)A1 A2 (N-1)A2 J0 (N-1)Z0
B1 (N-1)* E1 (N-1)* F1 (N-1)*
D1 (N-1)* D2 (N-1)* D3 (N-1)*
H1 (N-1)H1c H2 (N-1)H2c H3 (N-1)H3
B2 (N-1)B2 K1 (N-1)* K2 (N-1)*
D4 (N-1)* D5 (N-1)* D6 (N-1)*
D7 (N-1)* D8 (N-1)* D9 (N-1)*
D10 (N-1)* D11 (N-1)* D12 (N-1)*
S1 (N-1)Z1 (N-1)Z2,M1 E2 (N-1)*
STM-N
containing a VC-4-Xc
Section Overhead
N*9 bytes/row
9 rows
Path Overhead, Fixed Stuff and Data
N*261 bytes/row
9 rows
Key
Hnc
Concatenation pointer
(N-1)*
N-1 Undefined overhead bytes
(N-1)Z2,M1
The M1 byte is always in the third location

FIG. 17

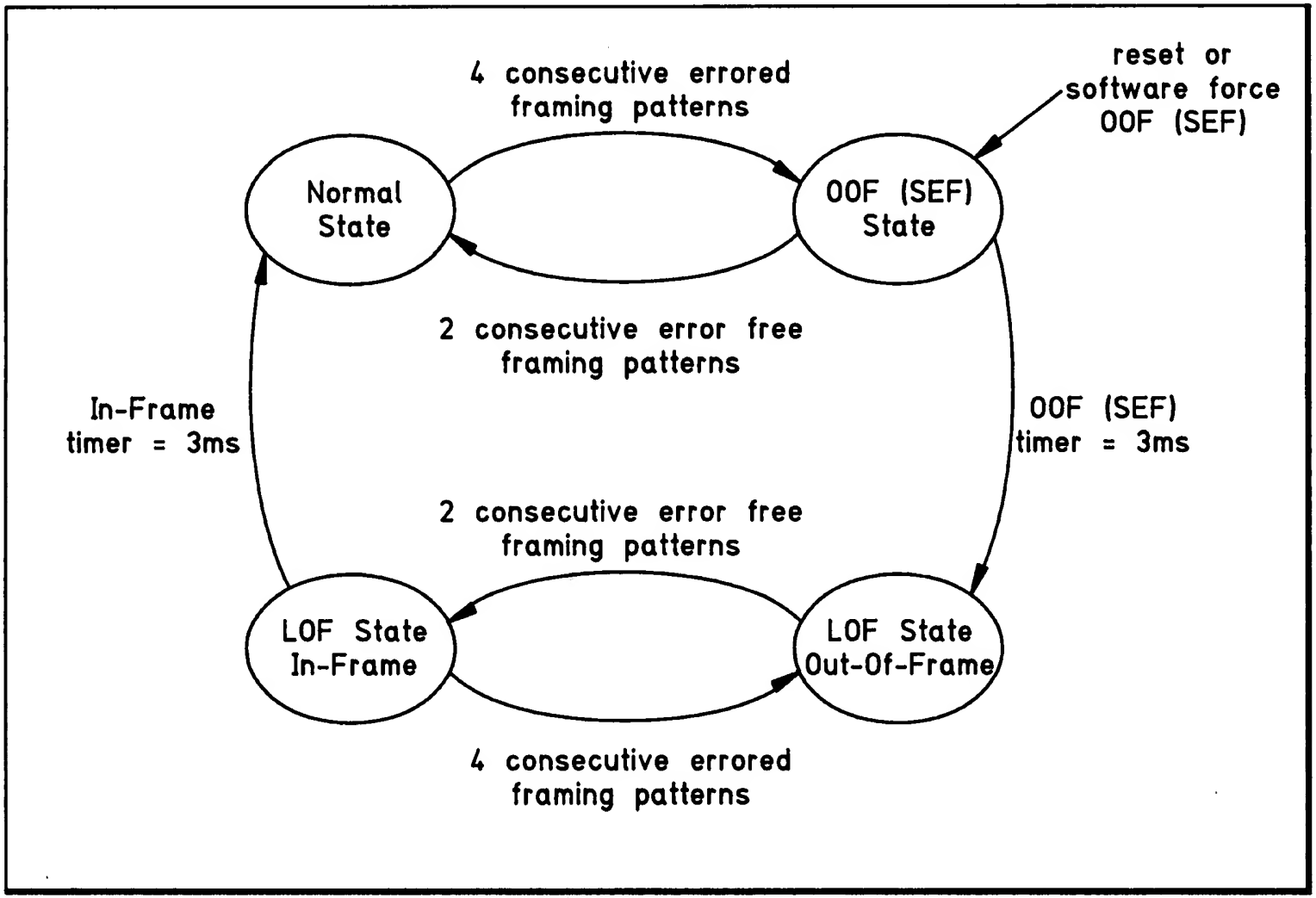
4 consecutive errored framing patterns
reset or software force OOF (SEF)
Normal State
OOF (SEF) State
2 consecutive error free framing patterns
In-Frame timer = 3ms
OOF (SEF) timer = 3ms
2 consecutive error free framing patterns
LOF State In-Frame
LOF State Out-Of-Frame
4 consecutive errored framing patterns

FIG. 18

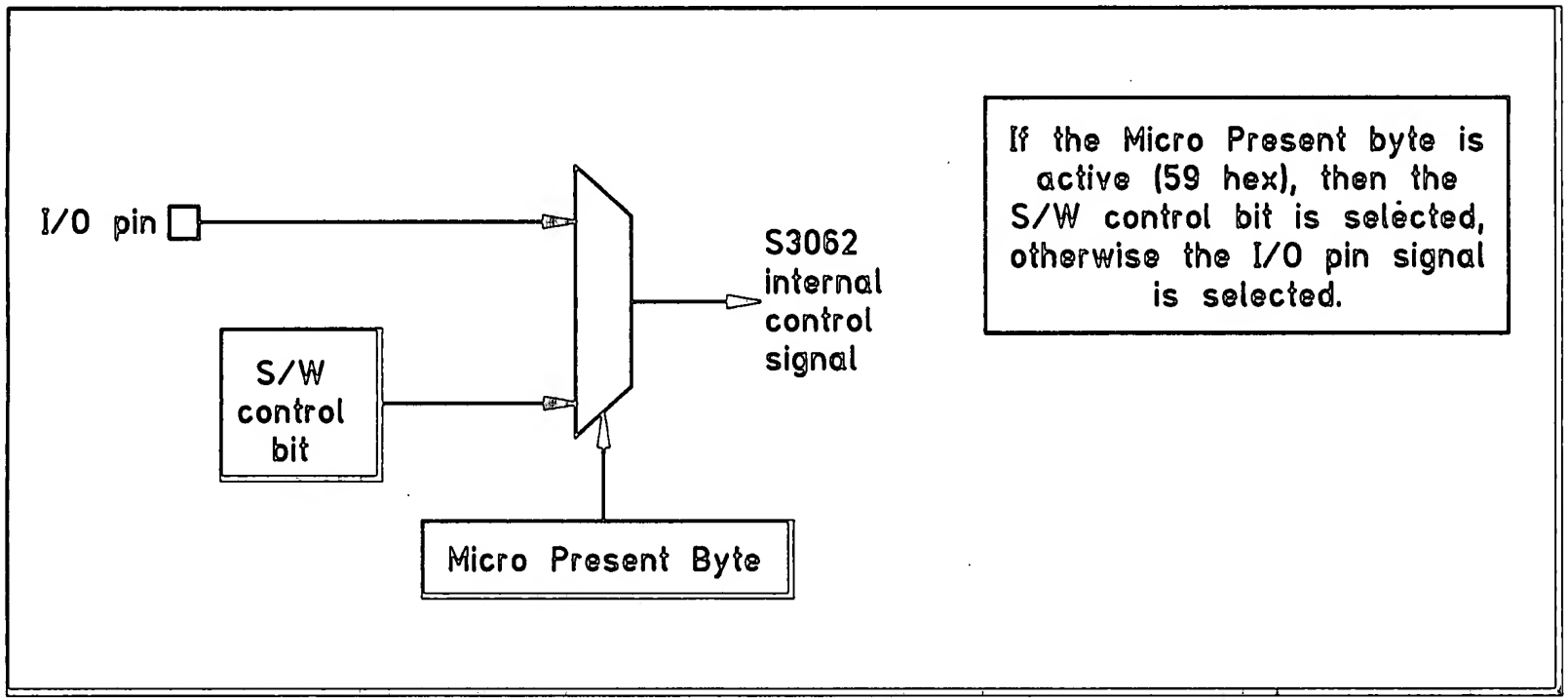
I/O pin
S/W control bit
S3062 internal control signal
Micro Present Byte
If the Micro Present byte is active (59 hex), then the S/W control bit is selected, otherwise the I/O pin signal is selected.

FIG. 19